Chapter 8
Ion Implantation

Wafer Process Flow
Introduction

• Semiconductor doping in wells and S/D
• Two major ways to dope
  – Diffusion
  – Ion implantation
• Other application of ion implantation

Semiconductor Doping: Diffusion

• An isotropic process
• Can’t independently control dopant profile and dopant concentration
• Replaced by ion implantation after its introduction in mid-1970s.
• Performed in high temperature furnace
• Using silicon dioxide as hard mask
• Still used for dopant drive-in, low-end product applications
• Current R&D on ultra shallow junction formation.

Dopant Oxide Deposition (or Pre-deposition)
Oxidation

SiO$_2$

Si Substrate

Drive-in

SiO$_2$

Doped junction

Si Substrate
Strip and Clean

Semiconductor Doping:
Ion Implantation

- First used for atomic and nuclear research
- Early idea introduced in 1950’s
- Introduced to semiconductor manufacturing in mid-1970s.
- Independently control dopant profile (ion energy) and dopant concentration (ion current times implantation time)
• Anisotropic dopant profile
• Easy to achieve high concentration dope of heavy dopant atom such as phosphorus and arsenic.

Misalignment of the Gate

Aligned

Misaligned
Ion Implantation, Phosphorus

Comparison of Implantation and Diffusion
Comparison of Implantation and Diffusion

<table>
<thead>
<tr>
<th>Diffusion</th>
<th>Ion Implantation</th>
</tr>
</thead>
<tbody>
<tr>
<td>Unable to achieve high dopant concentrations</td>
<td>Wide range of dopant dose (10^{11}~10^{17} atoms/cm²)</td>
</tr>
<tr>
<td>High temperature, hard mask</td>
<td>Low temperature, photoresist mask</td>
</tr>
<tr>
<td>Isotropic dopant profile</td>
<td>Anisotropic dopant profile</td>
</tr>
<tr>
<td>Cannot independently control of the dopant concentration and junction depth</td>
<td>Can independently control of the dopant concentration and junction depth</td>
</tr>
<tr>
<td>Batch process</td>
<td>Both Batch and single wafer process</td>
</tr>
</tbody>
</table>

Ion Implantation Control

- Beam current and implantation time control dopant concentration
- Ion energy controls junction depth
- Dopant profile is anisotropic
Other Applications

- Oxygen implantation for silicon-on-insulator (SOI) device
- Pre-amorphous silicon implantation on titanium film for better annealing
- Pre-amorphous germanium implantation on silicon substrate for profile control
- Polysilicon doping – poly barrier formation. Silicide on top of polysilicon shorts p-n junction of the silicon and forms local interconnection

Stopping Mechanism

- Ions penetrate into substrate
- Collide with lattice atoms
- Gradually lose their energy and stop

![Stopping Mechanism Diagram]
Two Stopping Mechanism

- Nuclear stopping
  - Collision with nuclei of the lattice atoms
  - Scattered significantly
  - Causes crystal structure damage.
- Electronic stopping
  - Collision with electrons of the lattice atoms
  - Incident ion path is almost unchanged
  - Energy transfer is very small
  - Crystal structure damage is negligible

Stopping Mechanism

- The total stopping power
  \[ S_{total} = S_n + S_e \]
- \( S_n \): nuclear stopping, \( S_e \): electronic stopping
- Low \( E \), high \( A \) ion implantation: mainly nuclear stopping
- High \( E \), low \( A \) ion implantation, electronic stopping mechanism is more important
Stopping Power and Ion Velocity

1. Nuclear Stopping
2. Electronic Stopping

Ion Trajectory and Projected Range

Distance to the Surface
Ion Projection Range

Projected Range in Silicon

Projected Range (µm)

Implantation Energy (keV)

Substrate Surface

Depth from the Surface

Projected Range

ln (Concentration)
Barrier Thickness to Block 200 keV Ion Beam

Implantation Processes: Channeling

- If the incident angle is right, ion can travel long distance without collision with lattice atoms
- It causes uncontrollable dopant profile, a tail
**Channeling Effect**

Channeling Ion

Collisional Ion

$\theta$

Wafer Surface

Lattice Atoms

**Post-collision Channeling**

Collisional Channeling Collisional

$\theta$

Wafer Surface

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Implantation Processes: Channeling

- Ways to avoid channeling effect
  - Tilt wafer, 7° is most commonly used
  - Screen oxide
  - Pre-amorphous implantation
- Shadowing effect
  - Ion blocked by structures
- Rotate wafer and post-implantation diffusion
Shadowing Effect

After Annealing and Diffusion
Damage Process

- Implanted ions transfer energy to lattice atoms
  - Atoms to break free
- Freed atoms collide with other lattice atoms
  - Free more lattice atoms
  - Damage continues until all freed atoms stop
- One energetic ion can cause thousands of displacements of lattice atoms

Lattice Damage With One Ion

- Light Ion
- Heavy Ion

Single Crystal Silicon

Damaged Region
Implantation Processes: Damage

- Ion collides with lattice atoms and knock them out of lattice grid
- Implant area on substrate becomes amorphous structure

![Before Implantation](image1.png) ![After Implantation](image2.png)

Implantation Processes: Anneal

- Dopant atom must in single crystal structure and bond with four silicon atoms to be activated as donor (N-type) or acceptor (P-type)
- Thermal energy from high temperature helps amorphous atoms to recover single crystal structure.
Thermal Annealing

Lattice Atoms
Dopant Atom

Thermal Annealing

Lattice Atoms
Dopant Atom
Thermal Annealing

Lattice Atoms

Dopant Atom

Thermal Annealing

Lattice Atoms

Dopant Atom
Thermal Annealing

Dopant Atom
Lattice Atoms

Thermal Annealing

Lattice Atoms
Dopant Atoms

2006/5
Implantation Processes: Annealing

Before Annealing

After Annealing

Rapid Thermal Annealing (RTA)

- At high temperature, annealing out pace diffusion
- Rapid thermal process (RTP) is widely used for post-implantation anneal
- RTA is fast (less than a minute), better WTW uniformity, better thermal budget control, and minimized the dopant diffusion
RTP and Furnace Annealing

Ion Implantation: Hardware

- Gas system
- Electrical system
- Vacuum system
- Ion beamline
Ion Implanter

Ion Implantation: Beamline

- Ion source
- Extraction electrode
- Analyzer magnet
- Post acceleration
- Plasma flooding system
- End analyzer
• Hot tungsten filament emits thermal electron
• Electrons collide with source gas molecules to dissociate and ionize
• Ions are extracted out of source chamber and accelerated to the beamline
• RF and microwave power can also be used to ionize source gas
**Ion Source**

- **Arc Power**: ~120 V
- **Filament Power**: 0-5V, up to 200A
- **Tungsten Filament**
- **Source Gas or Vapor**
- **Anticathode**
- **Magnetic Field Line**
- **Source Magnet**

**RF Ion Source**

- **Dopant Gas**
- **RF Coils**
- **Plasma**
- **RF**
- **Extraction Electrode**
- **Ion Beam**
Microwave Ion Source

Ion Implantation: Extraction

- Extraction electrode accelerates ions up to 50 keV
- High energy is required for analyzer magnet to select right ion species.
Ion Implantation: Analyzer Magnet

- Gyro radius of charge particle in magnetic field relate with B-field and mass/charge ratio
- Used for isotope separation to get enriched $\text{U}_{235}$
- Only ions with right mass/charge ratio can go through the slit
- Purified the implanting ion beam
Analyzer

Magnetic Field (Point Outward)

Ion Beam

Larger m/q Ratio

Flight Tube

Smaller m/q Ratio

Right m/q Ratio

Ions in BF$_3$ Plasma

<table>
<thead>
<tr>
<th>Ions</th>
<th>Atomic or molecule weight</th>
</tr>
</thead>
<tbody>
<tr>
<td>$^{10}$B</td>
<td>10</td>
</tr>
<tr>
<td>$^{11}$B</td>
<td>11</td>
</tr>
<tr>
<td>$^{10}$BF</td>
<td>29</td>
</tr>
<tr>
<td>$^{11}$BF</td>
<td>30</td>
</tr>
<tr>
<td>F$_2$</td>
<td>38</td>
</tr>
<tr>
<td>$^{10}$BF$_2$</td>
<td>48</td>
</tr>
<tr>
<td>$^{11}$BF$_2$</td>
<td>49</td>
</tr>
</tbody>
</table>
Ion Implantation: Post Acceleration

- Increasing (sometimes decreasing) ion energy for ion to reach the required junction depth determined by the device
- Electrodes with high DC voltage
- Adjustable vertical vanes control beam current

Ion Implantation: Plasma Flooding System

- Ions cause wafer charging
- Wafer charging can cause non-uniform doping and arcing defects
- Elections are “flooding” into ion beam and neutralized the charge on the wafer
- Argon plasma generated by thermal electrons emit from hot tungsten filament
Post Acceleration

Suppression Electrode

Acceleration Electrode

Terminal Chassis

Suppression Power, up to 10 kV

Post Accel. Power, up to 60 kV

Ion Beam Current Control

Fixed Defining Aperture

Adjustable Vertical Vanes

Ion Beam
Bending Ion Trajectory

Charge Neutralization System

- Implanted ions charge wafer positively
- Cause wafer charging effect
- Expel positive ion, cause beam blowup and result non-uniform dopant distribution
- Discharge arcing create defects on wafer
- Breakdown gate oxide, low yield
- Need eliminate or minimize charging effect
Charging Effect

Charge Neutralization System

• Need to provide electrons to neutralize ions
  – Plasma flooding system
  – Electron gun
  – Electron shower are used to
Plasma Flooding System

Electron Gun
Ion Implantation: The Process

- CMOS applications
- CMOS ion implantation requirements
- Implantation process evaluations
CMOS Implantation Requirements

<table>
<thead>
<tr>
<th>Implant Step</th>
<th>0.35 (\mu m), 64 Mb</th>
<th>0.25 (\mu m), 256 Mb</th>
<th>0.18 (\mu m), 1 Gb</th>
</tr>
</thead>
<tbody>
<tr>
<td>N-well</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Well</td>
<td>P/60/2\times10^{13}</td>
<td>P/40/2\times10^{13}</td>
<td>P/30/1\times10^{13}</td>
</tr>
<tr>
<td>Anti-punch through</td>
<td>P/100/5\times10^{13}</td>
<td>As/100/5\times10^{13}</td>
<td>As/50/2\times10^{13}</td>
</tr>
<tr>
<td>Threshold</td>
<td>B/10/7\times10^{13}</td>
<td>B/5/3\times10^{13}</td>
<td>B/2/4\times10^{13}</td>
</tr>
<tr>
<td>Poly dope</td>
<td>P/30/2\times10^{13}</td>
<td>B/20/2\times10^{13}</td>
<td>B/20/3\times10^{13}</td>
</tr>
<tr>
<td>Poly diffusion block</td>
<td>-</td>
<td>-</td>
<td>N_z/20/3\times10^{13}</td>
</tr>
<tr>
<td>Lightly doped drain (LDD)</td>
<td>B/7/5\times10^{13}</td>
<td>B/5/1\times10^{13}</td>
<td>B/2/8\times10^{13}</td>
</tr>
<tr>
<td>Halo (45° implant)</td>
<td>-</td>
<td>-</td>
<td>As/30/5\times10^{13}</td>
</tr>
<tr>
<td>Source/drain contact</td>
<td>B/10/2\times10^{13}</td>
<td>B/7/2\times10^{13}</td>
<td>B/6/2\times10^{13}</td>
</tr>
<tr>
<td>P-well</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Well</td>
<td>B/225/3\times10^{13}</td>
<td>B/200/1\times10^{13}</td>
<td>B/175/1\times10^{13}</td>
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<tr>
<td>Anti-punch through</td>
<td>B/50/2\times10^{13}</td>
<td>B/50/5\times10^{13}</td>
<td>B/4/5\times10^{13}</td>
</tr>
<tr>
<td>Threshold</td>
<td>B/10/7\times10^{13}</td>
<td>B/5/3\times10^{13}</td>
<td>B/2/4\times10^{13}</td>
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<tr>
<td>Poly dope</td>
<td>P/30/5\times10^{13}</td>
<td>P/20/2\times10^{13}</td>
<td>As/40/3\times10^{13}</td>
</tr>
<tr>
<td>Poly diffusion block</td>
<td>-</td>
<td>-</td>
<td>N_z/20/3\times10^{13}</td>
</tr>
<tr>
<td>Lightly doped drain (LDD)</td>
<td>P/20/5\times10^{13}</td>
<td>P/12/5\times10^{13}</td>
<td>P/5/3\times10^{13}</td>
</tr>
<tr>
<td>Halo (45° implant)</td>
<td>B/30/3\times10^{12}</td>
<td>B/20/3\times10^{12}</td>
<td>B/7/2\times10^{12}</td>
</tr>
<tr>
<td>Source/drain contact</td>
<td>As/30/3\times10^{13}</td>
<td>As/20/3\times10^{13}</td>
<td>As/15/3\times10^{13}</td>
</tr>
</tbody>
</table>

Implantation Process: Well Implantation

- High energy (to MeV), low current (\(10^{13}/\text{cm}^2\))

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Implantation Process: $V_T$ Adjust Implantation

Low Energy, Low Current

Lightly Doped Drain (LDD) Implantation

- Low energy (10 keV), low current ($10^{13}$/cm$^2$)
Implantation Process: S/D Implantation

- Low energy (20 keV), high current (>10^{15}/cm^2)

Ion Implantation Processes

<table>
<thead>
<tr>
<th>Ion Implantation</th>
<th>Energy</th>
<th>Current</th>
</tr>
</thead>
<tbody>
<tr>
<td>Well</td>
<td>High energy</td>
<td>low current</td>
</tr>
<tr>
<td>Source/Drain</td>
<td>Low energy</td>
<td>high current</td>
</tr>
<tr>
<td>V_T Adjust</td>
<td>Low energy</td>
<td>low current</td>
</tr>
<tr>
<td>LDD</td>
<td>Low energy</td>
<td>low current</td>
</tr>
</tbody>
</table>
Process Issues

- Wafer charging
- Particle contamination
- Elemental contamination
- Process evaluation

Wafer Charging

- Break down gate oxide
- Dielectric strength of SiO$_2$: $\sim$10 MV/cm
- 100 Å oxide breakdown voltage is 10 V
- Gate oxide: 30 to 35 Å for 0.18 µm device
- Require better charge neutralization
Wafer Charging Monitoring

- Antenna capacitor changing test structure
- The ratio of polysilicon pad area and thin oxide area is called antenna ratio
- Can be as high as 100,000:1
- The larger antenna ratio, the easier to breakdown the thin gate oxide
Particle Contamination

- Large particles can block the ion beam especially for the low energy processes,
- $V_T$ adjust, LDD and S/D implantations,
- Cause incomplete dopant junction.
- Harmful to yield

Effect of Particle Contamination
Elemental Contamination

- Co-implantation other elements with intended dopant
- $^{94}\text{Mo}^{++}$ and $^{11}\text{BF}_2^+$, same mass/charge ratio ($A/e = 49$)
- Mass analyzer can’t separate these two
- $^{94}\text{Mo}^{++}$ causes heavy metal contamination
- Ion source can’t use standard stainless steel
- Other materials such as graphite and tantalum are normally used

Process Evaluation

- Four-point probe
- Thermal wave
- Optical measurement system (OMS)
Thermal Wave System

• Argon “pump” laser generates thermal pulses on wafer surface
• He-Ne probe laser measures DC reflectivity ($R$) and reflectivity modulation induced by the pump laser ($\Delta R$) at the same spot
• Ratio $\Delta R/R$ is called thermal wave (TW) signal,
  – TW signal $\Delta R/R$ related to the crystal damage
  – crystal damage is a function of the implant dose
Thermal Wave System

- Performed immediately after the implant process
  - Four-point probe needs anneal first
- Non-destructive, can measure production wafers
  - Four-point probe is only good for test wafers
- Low sensitivity at low dosage
- Drift of the TW signal over time
  - needs to be taken as soon as the implantation finished
- Don’t have very high measurement accuracy
  - Laser heating relax crystal damage

Ion Implantation: Safety

- One of most hazardous process tools in semiconductor industry
- Chemical
- Electro-magnetic
- Mechanical
Ion Implantation: Chemical Safety

- Most dopant materials are highly toxic, flammable and explosive.
- Poisonous and explosive: AsH$_3$, PH$_3$, B$_2$H$_6$
- Corrosive: BF$_3$
- Toxic: P, B, As, Sb

- Common sense: get out first, let the trained people to do the investigation.

Ion Implantation: Electro-magnetic Safety

- High voltage: from facility 208 V to acceleration electrode up to 50 kV.
- Ground strip, Work with buddy!
- Lock & tag

- Magnetic field: pacemaker, etc.
Ion Implantation: Radiation Safety

- High energy ions cause strong X-ray radiation
- Normally well shielded

Ion Implantation: Corrosive by-products

- BF$_3$ as dopant gas
- Fluorine will react with hydrogen to form HF
- Anything in the beamline could have HF
- Double glove needed while wet clean those parts
Ion Implantation: Mechanical Safety

- Moving parts, doors, valves and robots
- Spin wheel
- Hot surface
- ......

Technology Trends

- Ultra shallow junction (USJ)
- Silicon on insulator (SOI)
- Plasma immersion ion implantation (PIII)
Ultra Shallow Junction (USJ)

- USJ ($x_j \leq 0.05 \mu m$) for sub-0.1 $\mu m$ devices
  - p-type junction, boron ion beam at extremely low energy, as low as 0.2 keV
- The requirements for the USJ
  - Shallow
  - Low sheet resistance
  - Low contact resistance
  - Minimal impact on channel profile
  - Compatible with polysilicon gate

CMOS on SOI Substrate

n$^+$ source/drain | Gate oxide | p$^+$ source/drain
---|---|---
p-Si | Polysilicon | s-Si
STI | Buried oxide | USG
Balk Si
SOI Formation

- Implanted wafers
  - Heavy oxygen ion implantation
  - High temperature annealing
- Bonded wafers
  - Two wafers
  - Grow oxide on one wafer
  - High temperature bond wafer bonding
  - Polish one wafer until thousand Å away from SiO₂

Oxygen Ion Implantation

- Silicon with lattice damage
- Oxygen rich silicon
- Balk Si
High Temperature Annealing

- Single crystal silicon
- Silicon dioxide
- Balk Si

Plasma Immersion Ion Implantation

- Deep trench capacitor for DRAM
- Deeper and narrower
- Very difficult to heavily dope both sidewall and bottom by ion implantation
- Plasma immersion ion implantation (PIII)
- An ion implantation process without precise ion species and ion energy selection
Deep Trench Capacitor

- Polysilicon
- Dielectric Layer
- Heavily doped Si
- Silicon Substrate

ECR Plasma Immersion System

- Microwave
- Magnet Coils
- Magnetic field line
- E-chuck
- Bias RF
- Helium
Summary of Ion Implantation

• Dope semiconductor
• Better doping method than diffusion
• Easy to control junction depth (by ion energy) and dopant concentration (by ion current and implantation time).
• Anisotropic dopant profile.

Summary of Ion Implantation

• Ion source
• Extraction
• Analyzer magnets
• Post acceleration
• Charge neutralization system
• Beam stop
Summary of Ion Implantation

- Well: High energy, low current
- Source/Drain: Low energy, high current
- Vt Adjust: Low energy, low current
- LDD: Low energy, low current